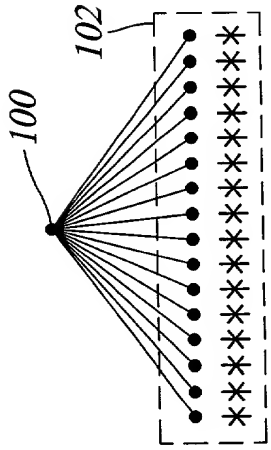


FIG. 1

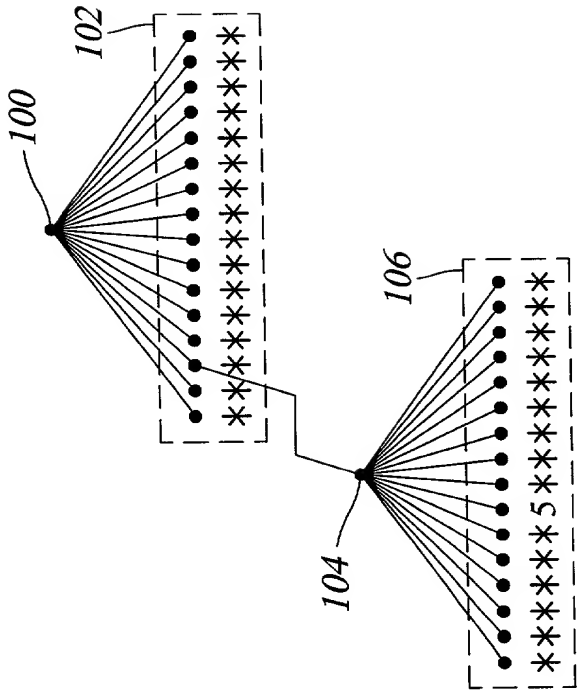


FIG. 2

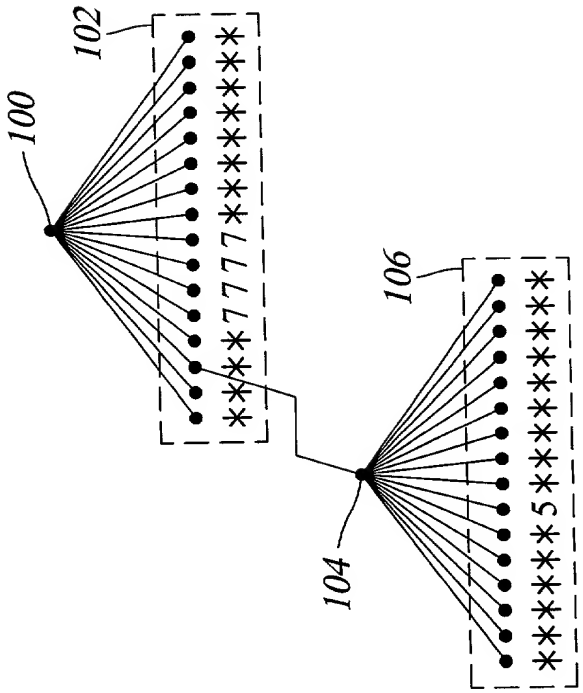


FIG. 3

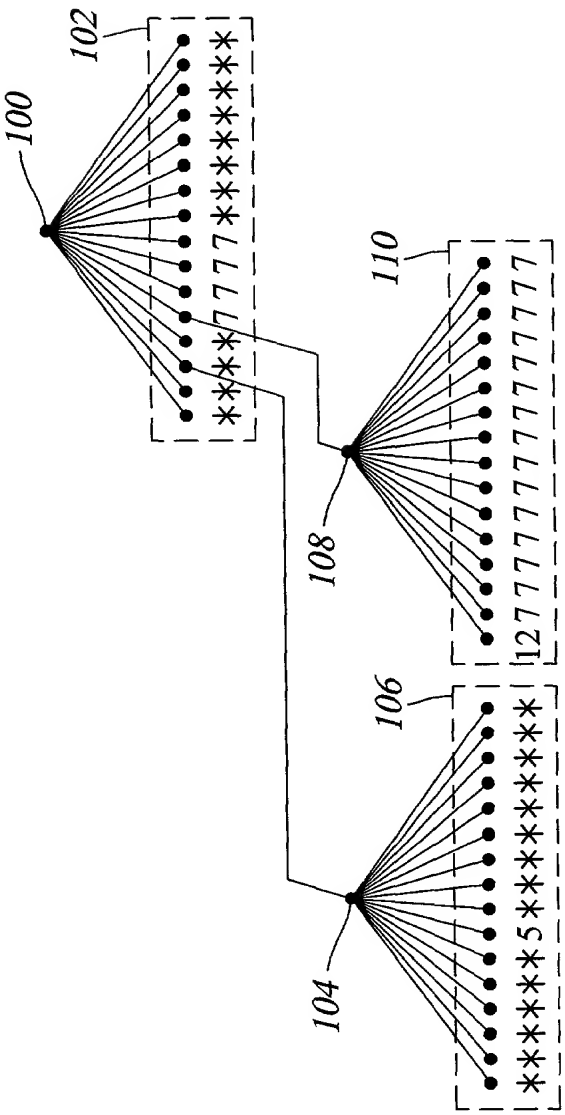


FIG. 4

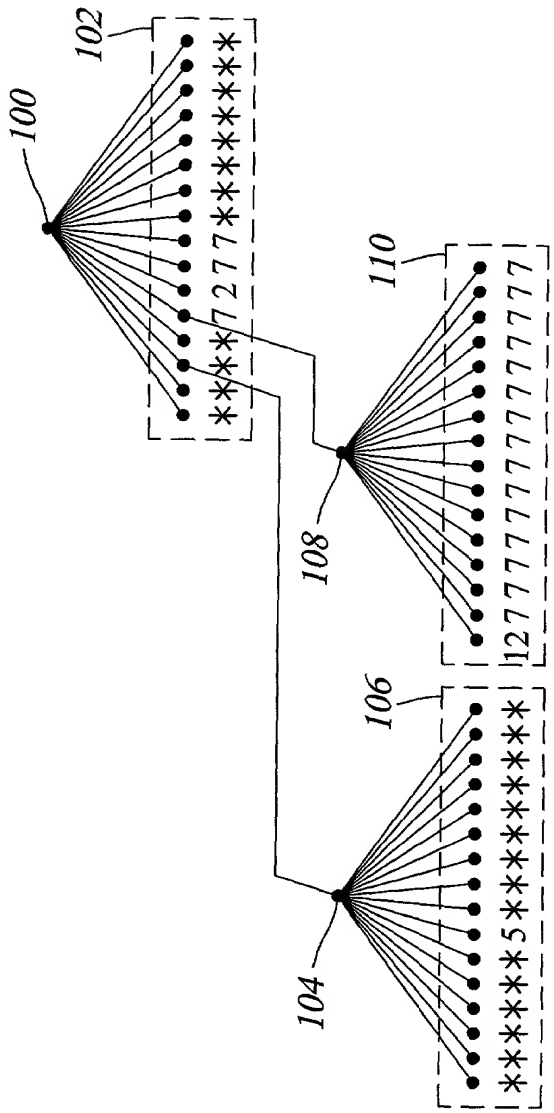


FIG. 5

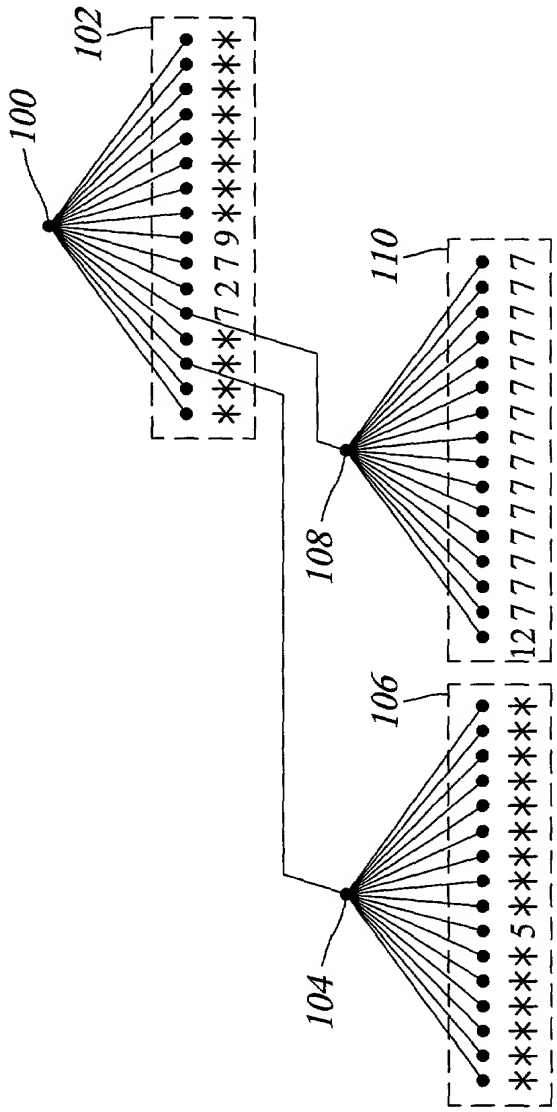


FIG. 6

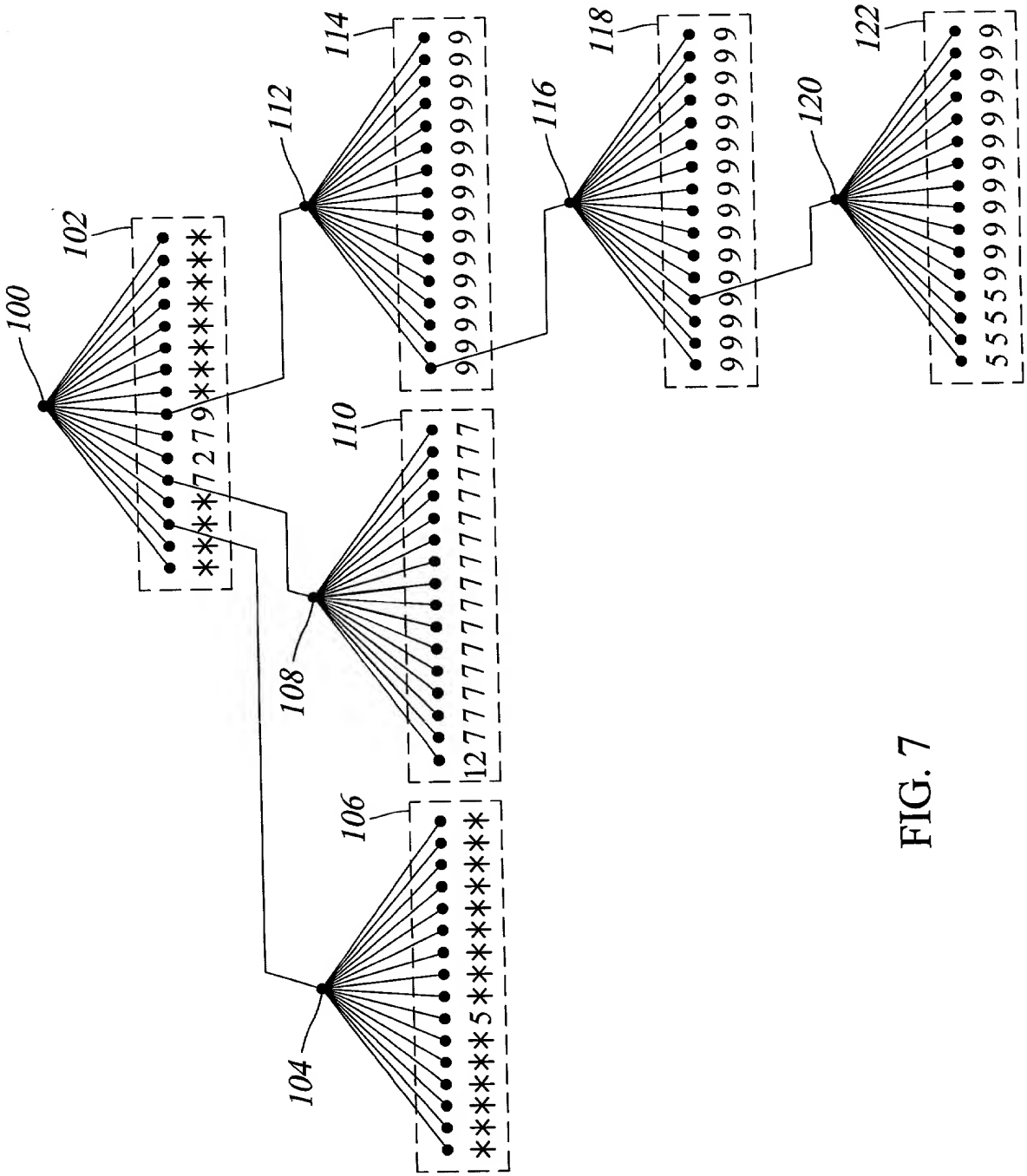
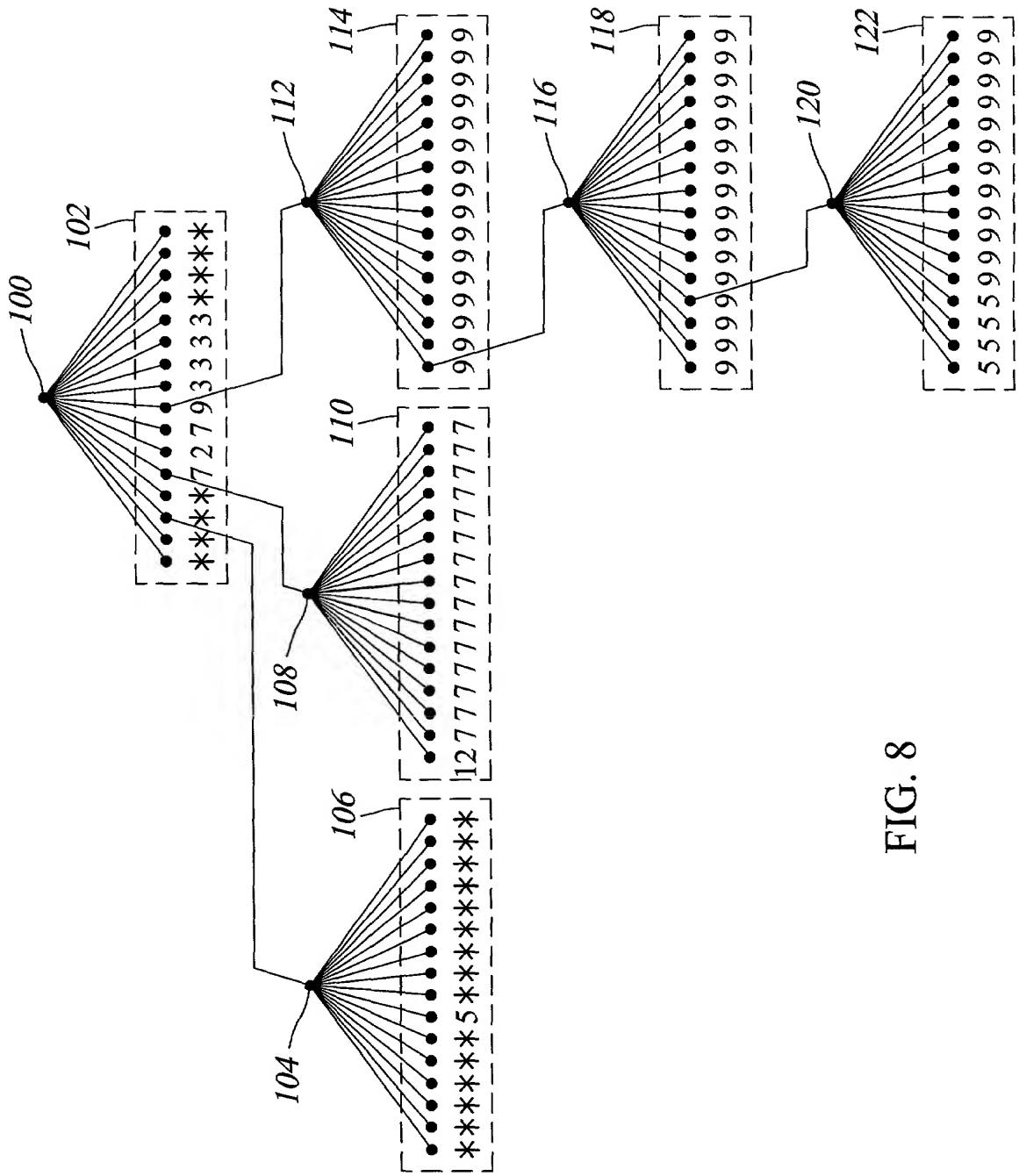

100
102
112
114
116
118
120
122
110
108
106
104
99999999999999
999999999999999
55559999999999999

FIG. 7


100
102
112
114
116
118
120
122
110
108
106
104
****
*****
*****
*****

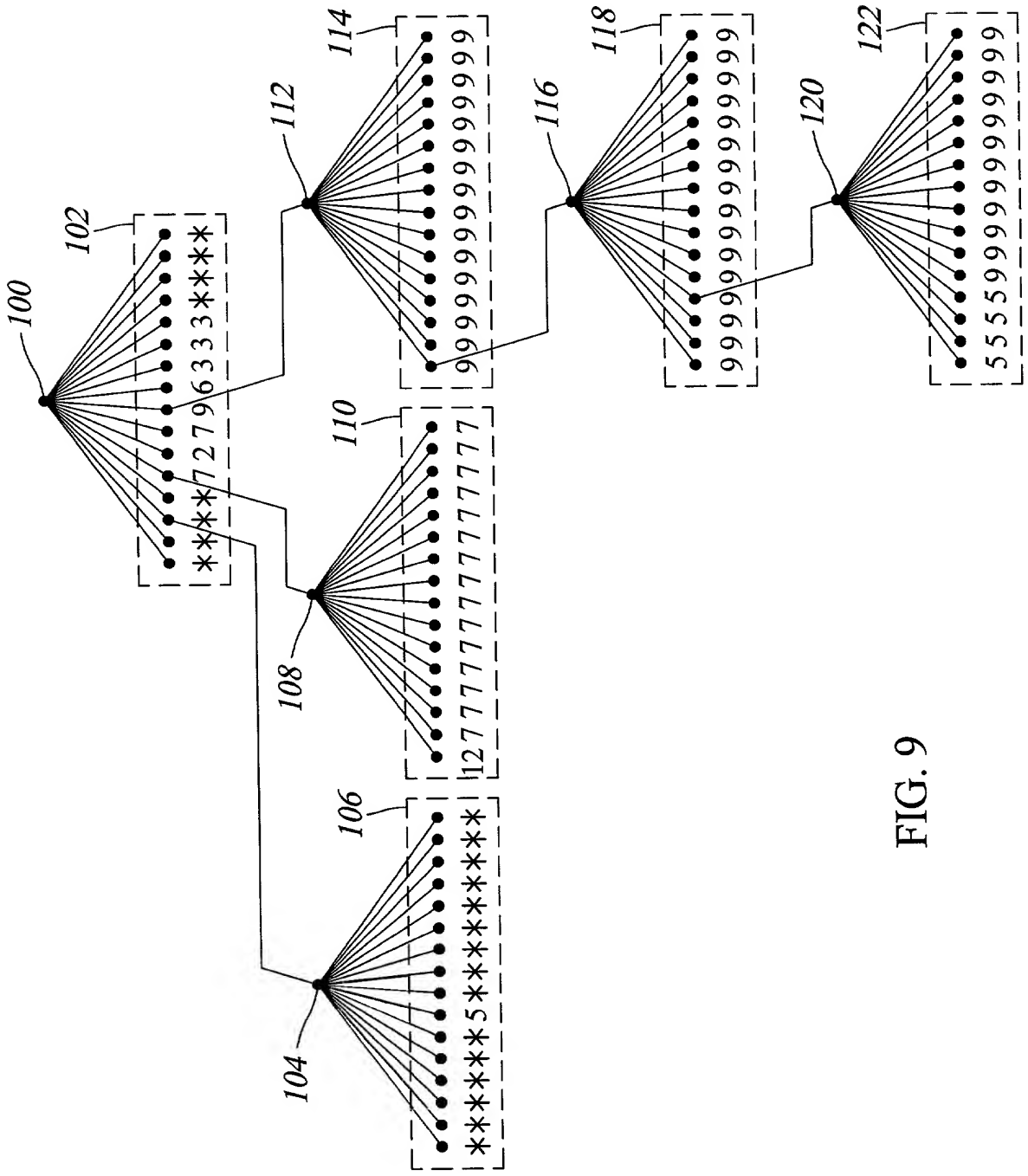

100
102
*****7279633****
104
*****5*********
106
****
108
127777777777777
110
112
999999999999
114
116
999999999999
118
120
555599999999999
122

FIG. 9

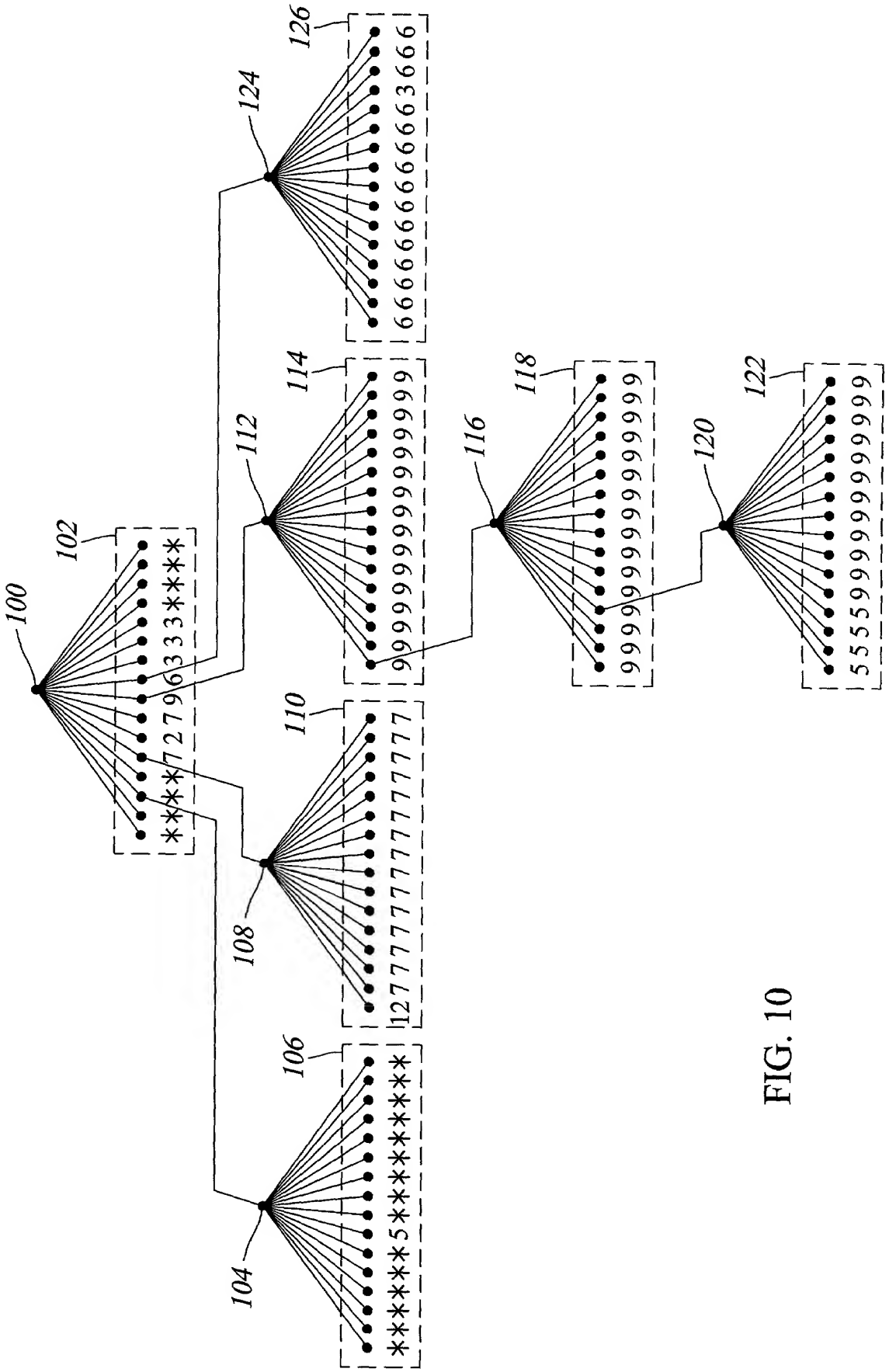


FIG. 10

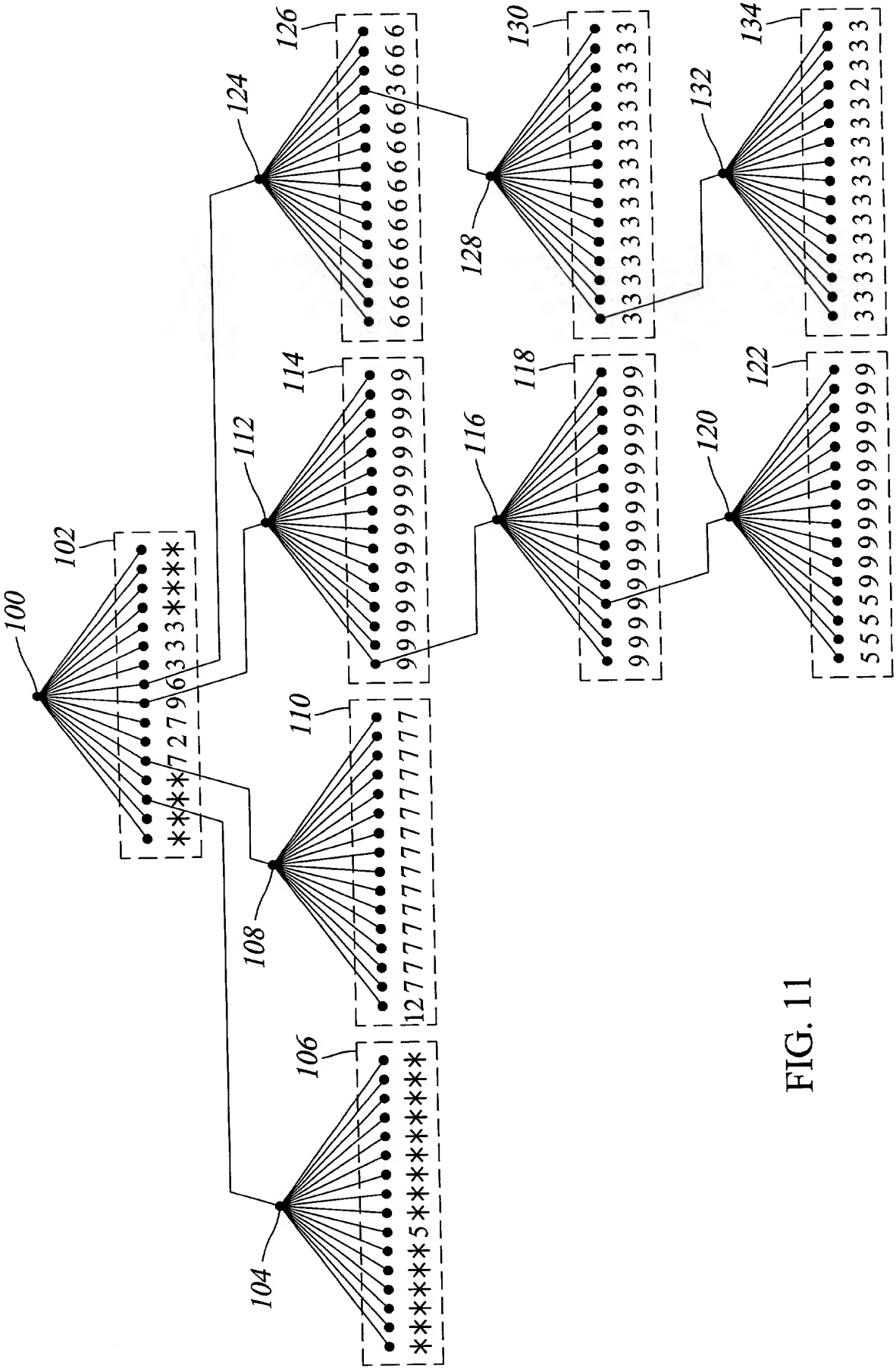

100
102
27963
104
*****5*********
106
12777777777777
108
110
99999999999999
112
114
66666666666663
124
126
33333333333333
128
130
99999999999999
116
118
55599999999999
120
122
33333333333333
132
134

FIG. 11

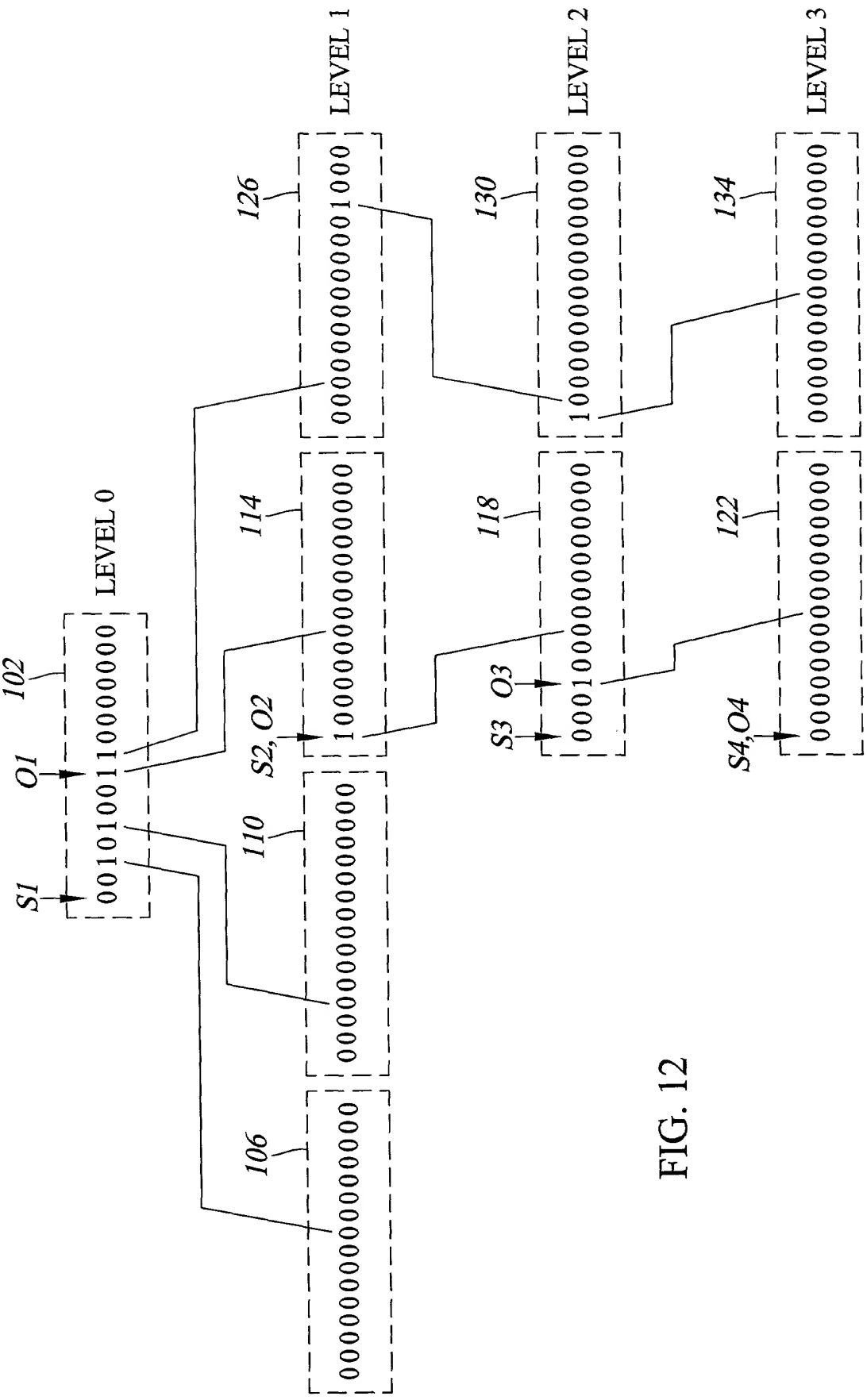

LEVEL 0
LEVEL 1
LEVEL 2
LEVEL 3
S1
O1
102
00101001100000000
106
0000000000000000
S2, O2
114
1000000000000000
110
0000000000000000
S3 O3
118
0001000000000000
122
0000000000000000
S4,O4
126
0000000000001000
130
1000000000000000
134
0000000000000000

FIG. 12

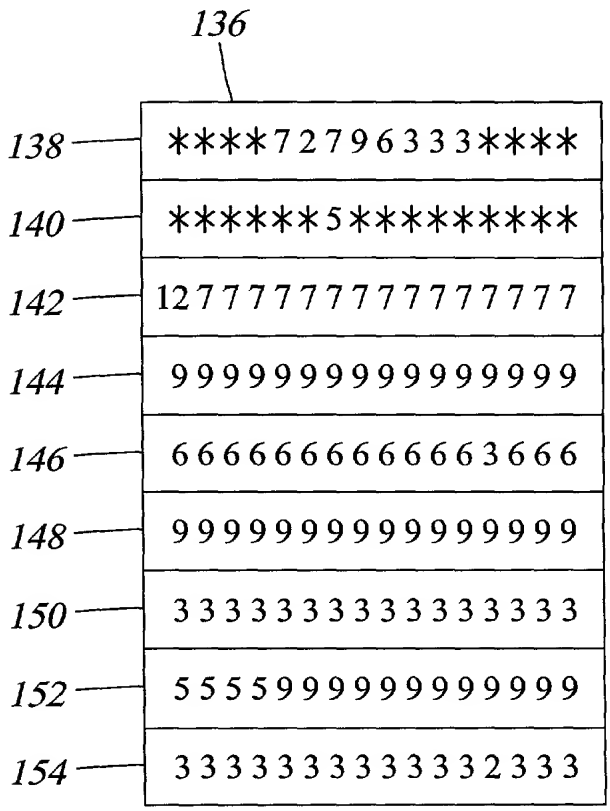

136
138
****72796333****
140
******5*********
142
12777777777777777
144
9999999999999999
146
6666666666663666
148
9999999999999999
150
3333333333333333
152
5555999999999999
154
3333333333332333

FIG. 13

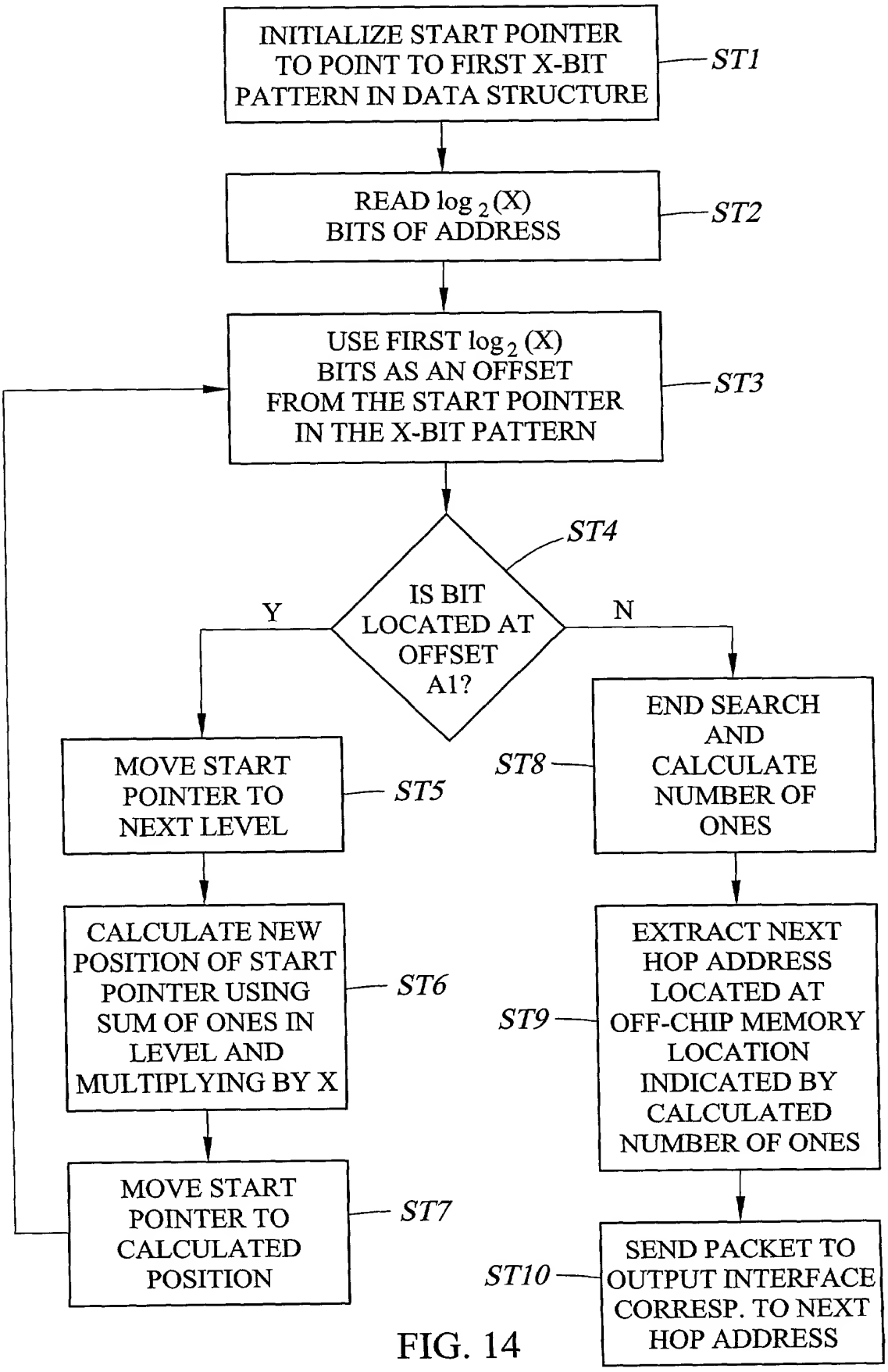

INITIALIZE START POINTER TO POINT TO FIRST X-BIT PATTERN IN DATA STRUCTURE
ST1
READ log 2 (X) BITS OF ADDRESS
ST2
USE FIRST log 2 (X) BITS AS AN OFFSET FROM THE START POINTER IN THE X-BIT PATTERN
ST3
ST4
IS BIT LOCATED AT OFFSET A1?
Y
N
MOVE START POINTER TO NEXT LEVEL
ST5
CALCULATE NEW POSITION OF START POINTER USING SUM OF ONES IN LEVEL AND MULTIPLYING BY X
ST6
MOVE START POINTER TO CALCULATED POSITION
ST7
END SEARCH AND CALCULATE NUMBER OF ONES
ST8
EXTRACT NEXT HOP ADDRESS LOCATED AT OFF-CHIP MEMORY LOCATION INDICATED BY CALCULATED NUMBER OF ONES
ST9
SEND PACKET TO OUTPUT INTERFACE CORRESP. TO NEXT HOP ADDRESS
ST10

FIG. 14

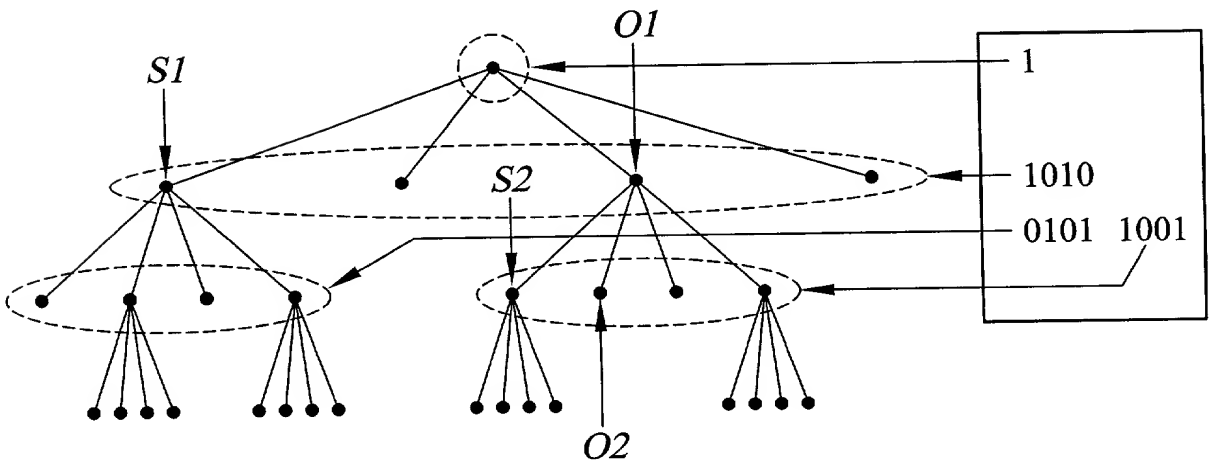


FIG. 15A

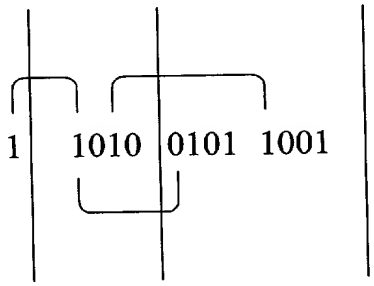


FIG. 15B

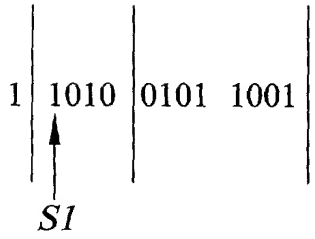


FIG. 16

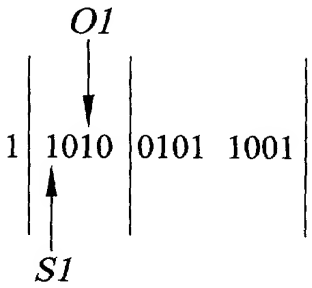


FIG. 17

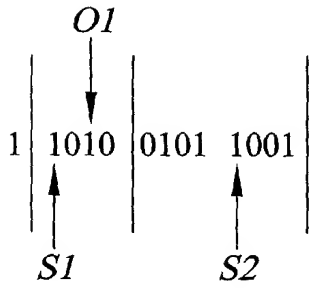


FIG. 18

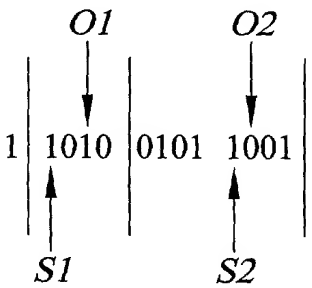


FIG. 19

Sum	Bit Pattern	
0x0000	0x2980	Level 0
0x0000	0x0000 0x0000 0x8000 0x0008	Level 1
0x0000	0x1000 0x8000	Level 2
0x0000	0x0000 0x0000	Level 3

FIG. 20

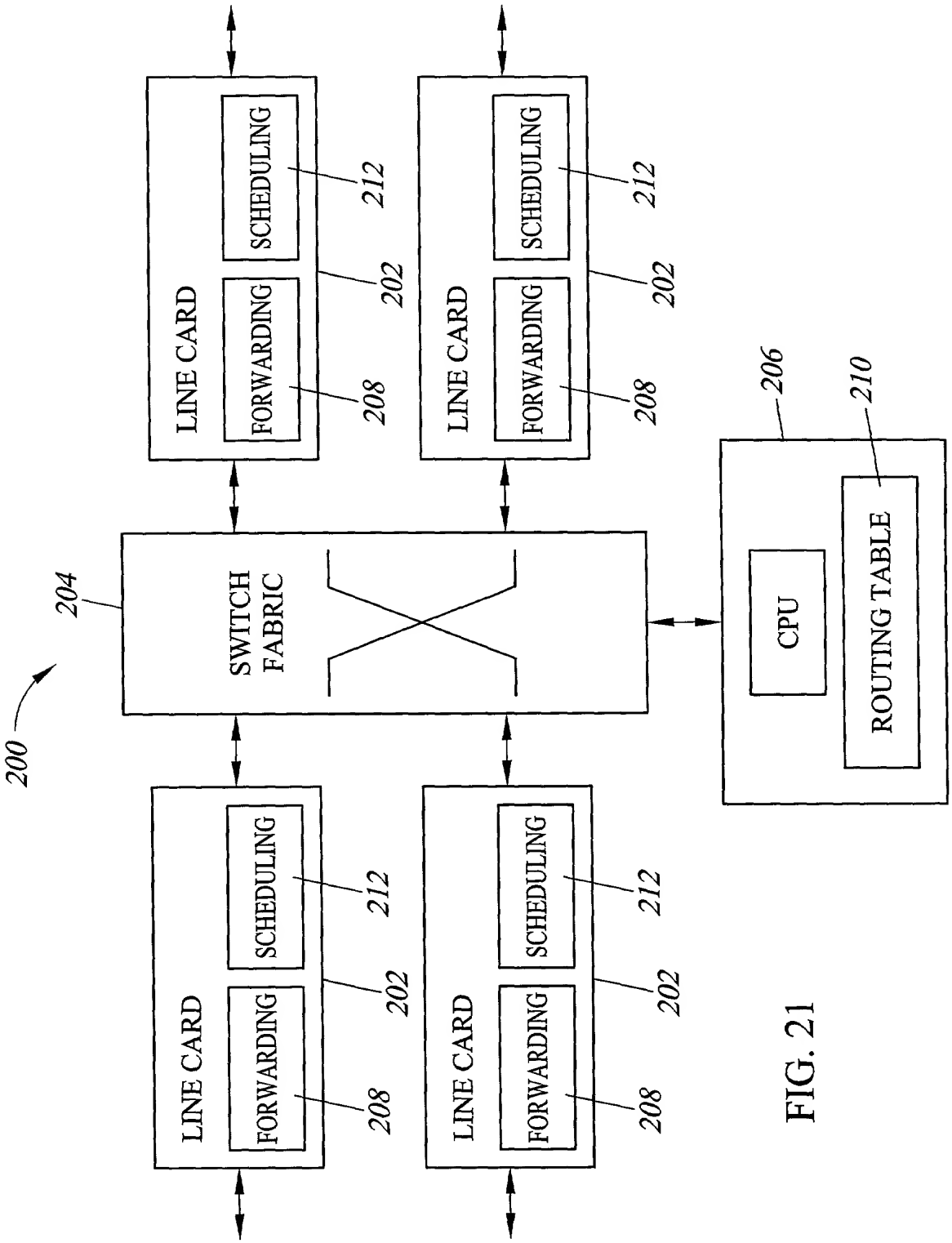

200
204
SWITCH FABRIC
LINE CARD
FORWARDING
SCHEDULING
202
208
212
206
CPU
ROUTING TABLE
210

FIG. 21

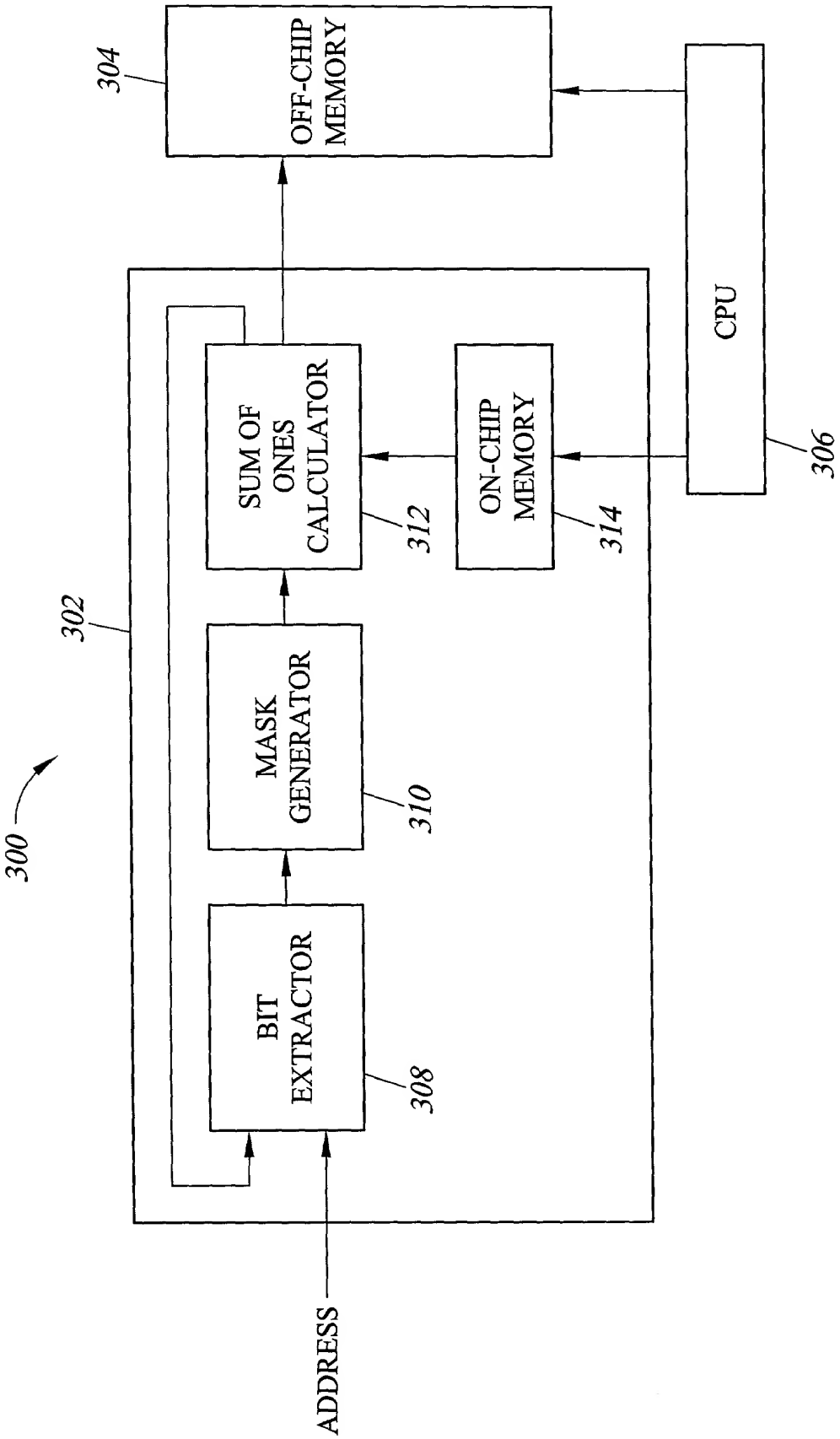

300
302
304
OFF-CHIP MEMORY
CPU
306
SUM OF ONES CALCULATOR
312
ON-CHIP MEMORY
314
MASK GENERATOR
310
BIT EXTRACTOR
308
ADDRESS

FIG. 22

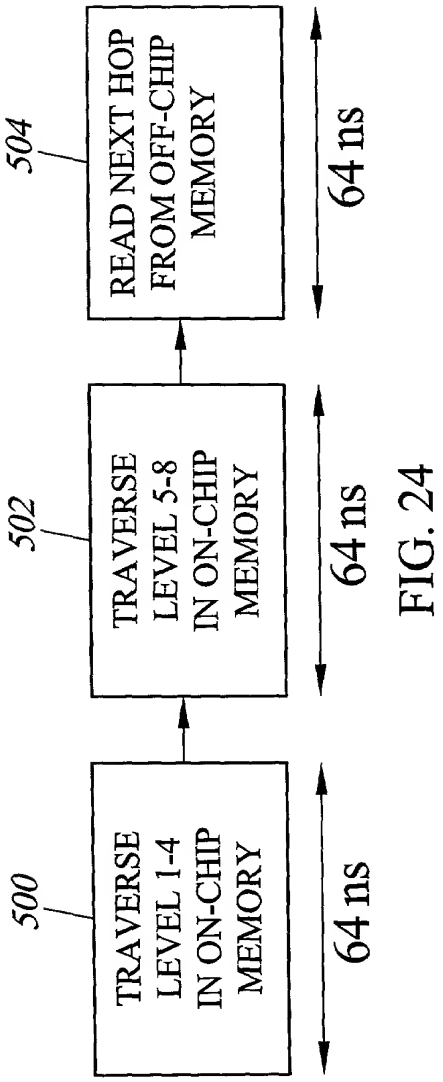


FIG. 24

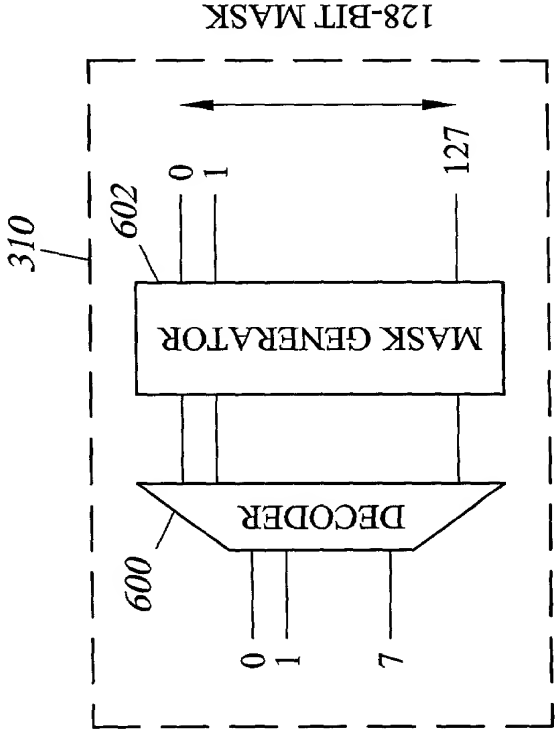


FIG. 25

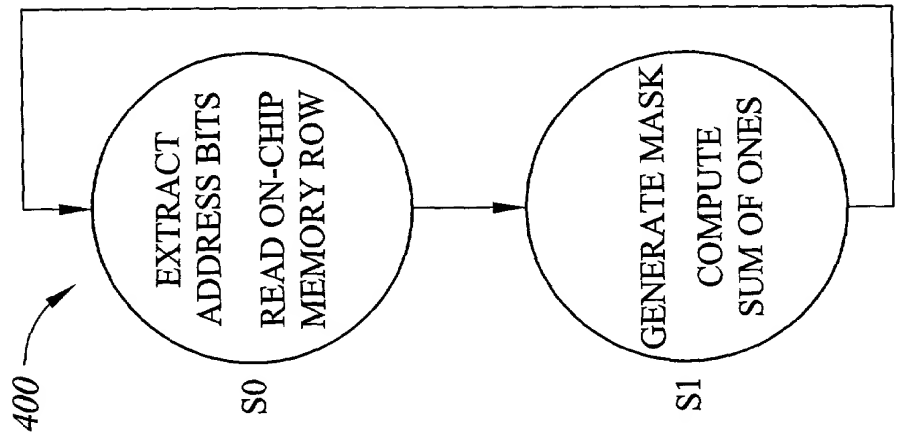


FIG. 23

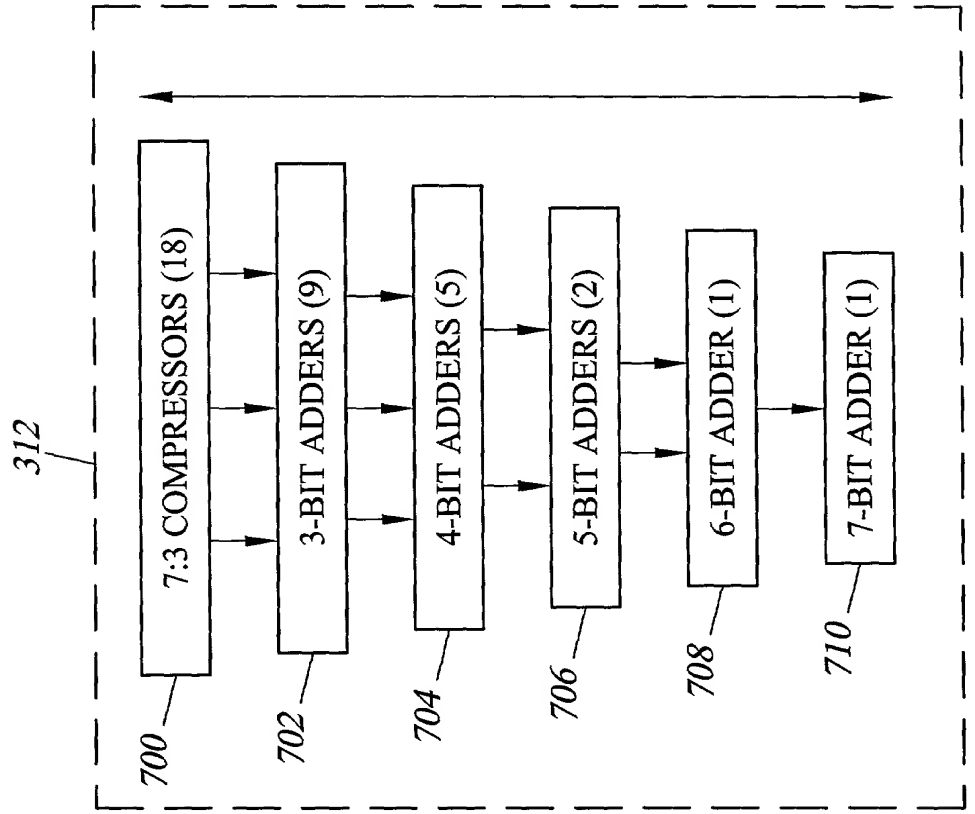

312
7:3 COMPRESSORS (18)
3-BIT ADDERS (9)
4-BIT ADDERS (5)
5-BIT ADDERS (2)
6-BIT ADDER (1)
7-BIT ADDER (1)
700
702
704
706
708
710

FIG. 27

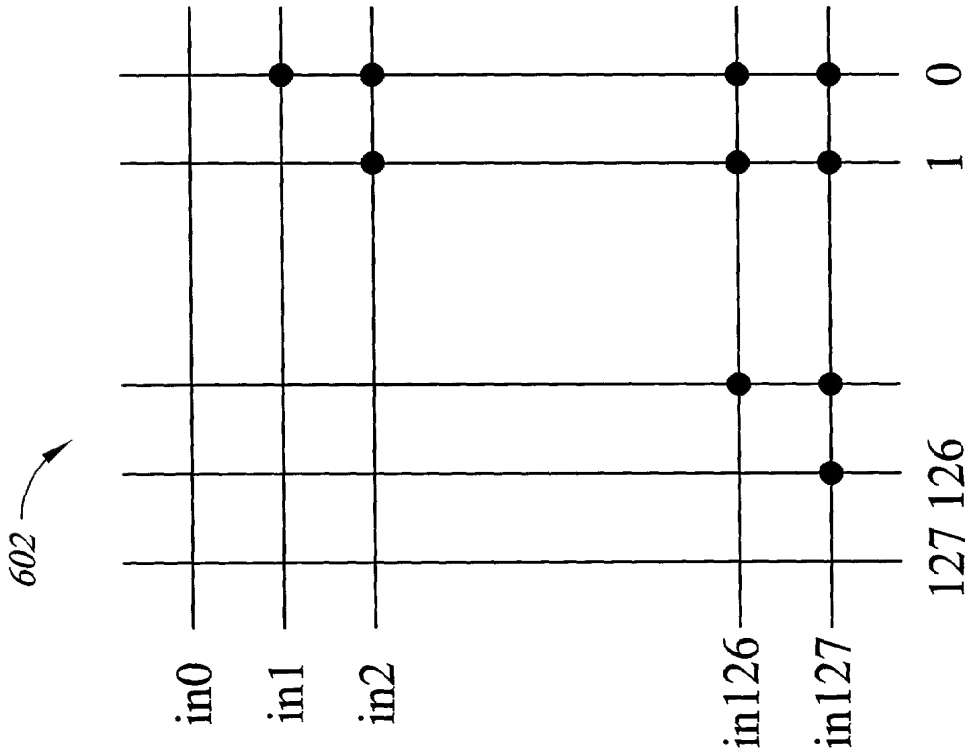

602
in0
in1
in2
in126
in127
127 126
1 0

FIG. 26